A Sub 1-V SOI CMOS Low Noise Amplifier for L-Band Applications

Hiroshi Komurasaki, Hisayasu Sato, Nagisa Sasaki,
Kimio Ueda, Shigenobu Maeda, Yasuo Yamaguchi, and Takahiro Miki
ULSI Laboratory, Mitsubishi Electric Corporation
4-1 Mizuhara, Itami, Hyogo 664-8641, Japan

ABSTRACT

This paper describes a sub 1.0 V low noise amplifier in a 0.35 µm SOI (silicon on insulator) CMOS process. Active-body control enables a sub 1.0 V operation, and improves gain and the 1 dB-compression point. The gain of 7.0 dB, the NF of 3.6 dB and the input 1 dB-compression point of -4.5 dBm are obtained at 1.0 V and 1.9 GHz.

INTRODUCTION

A number of MMICs have been designed and fabricated for microwave applications such as cellular phones and digital cordless phones [1-4]. In this type of wireless communication equipment, low costs and light weight are required. Silicon devices are better at achieving low costs than garium arsenide devices and CMOS technology is quite suitable for the integration of RF, IF and baseband. However, it has not been easy to use the silicon CMOS devices in L-band MMICs. Furthermore, lightweight phones need light batteries. Lowering the supply voltage is an effective way of reducing the battery weight. A lower supply voltage, such as a 1-cell battery (1.0-1.2 V), will be required for the next generation of wireless systems.

In this paper, a low noise amplifier for L-band applications with the supply voltage of sub 1.0 V is proposed.

SOI CMOS TECHNOLOGY

The SOI MOS device is one of the best candidates for high frequency applications because of its smaller parasitic capacitance at source and drain than that of bulk MOSs. Moreover, even at low voltage (below 1 V) SOI devices have high speed performance.

We use a 0.35 µm SOI CMOS technology for gate arrays [5]. This is the Field

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Shield (FS) isolated device for large scale applications. The FS-isolated MOSFET are fabricated as shown in Figure 1. The body of a MOSFET can be controlled by using the FS plate. The threshold voltage is 0.35 V and the f_{MAX} of an nMOSFET is more than 7 GHz with W_G (gate width) of 448 μm, V_{GS} (gate-source voltage) of 0.5 V and V_{DS} (drain-source voltage) of 1.0 V.

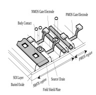

Figure 1 Oblique view of the Field Shield (FS) isolated gate array.

However, the SOI CMOS process is for gate arrays so it has no resistors or capacitors. Therefore we use parasitic elements to implement analog circuits. The resistor is the polysilicon FS plate and the capacitor is MOSFET gate capacitance. In order to obtain high capacitance in both the accumulation and inversion modes, we placed N+ and P+ electrodes next to the channel region. The capacitance per unit area is 4.7 fF/μm^2. In addition, the process has 2.5 μm-thick aluminum for the 3rd-layer aluminum to reduce the loss of on-chip spiral inductors.

CIRCUIT DESIGN AND FABRICATION

Figure 2 is a schematic of the proposed active-body type (AB type) low noise amplifier. The body of the transistor is connected to its gate. The threshold voltage of the transistor becomes smaller due to body effect so that a large drain current is obtained which keeps the gain high even at a lower supply voltage. An added feature of connection between the body and the gate is the high 1 dB-compression point. This is because the transistor can drive large load capacitance with a larger RF signal input due to the active threshold voltage of the body control.

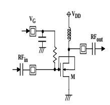

Figure 2 Active-Body type low noise amplifier.

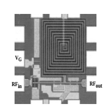

Figure 3 Photomicrograph of the AB type LNA chip

A photomicrograph of the AB type LNA is shown in Figure 3. The active area is 450 x 450 μm^2. The gate width of the transistor is 448 μm. The overall dimension of the load inductor is 350 μm, and the number of turns is 10. The line width and the spacing are 11 μm and 5 μm, respectively.

EXPERIMENTAL RESULTS

The results described in this paper are obtained from in-mold-package measurement employing tuner matching.

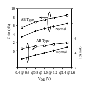

Figure 4 Dependence of gain on supply voltage

Figure 4 shows the supply-voltage dependence of the measurement gain and the drain current at V_G of 0.5 V. The results of a normal LNA, in which the body of the transistor is connected to the source, are also shown for comparison. The RF frequency is 1.9 GHz. The drain current of the AB type LNA can be kept larger than that of the normal type, so that a higher gain is achieved even at the supply voltage of 0.5 V. The gain is 5.5 dB at supply voltage of 0.5 V. This is 2.1 dB higher than that of the normal LNA.

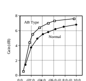

Figure 5 Dependence of gain on drain current

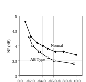

Figure 6 Dependence of NF on drain current

The relation between the drain current, I_d and the gain and NF at supply voltage of 1.0 V are shown in Figure 5 and Figure 6, respectively. The RF frequency is the same as mentioned above. A higher gain and a smaller NF than those of the normal LNA are obtained at the same current because of the active-body effect. The gain is higher by 1.2 dB and the NF is smaller by 0.3 dB at the same I_d of 5.0 mA.

TABLE I

Summary of experimental results

	Active Body Type LNA		Normal LNA
	Measured Value		Measured Value
Supply Voltage	0.5 V	1.0 V	1.0 V
Supply Current	4.6 mA	5.0 mA	5.0 mA
RF Frequency	1.9 GHz	1.9 GHz	1.9 GHz
Gain@NFmin	5.5 dB	7.0 dB	5.8 dB
NFmin	3.8 dB	3.6 dB	3.9 dB
P_{1dB} (input)	-10.8 dBm	-4.5 dBm	-6.2 dBm
IP3 (input)	-0.5 dBm	+6.0 dBm	+4.5 dBm

The measured characteristics are summarized in TABLE I. The supply voltages are 0.5 V and 1.0 V. The AB type LNA achieves a higher input 1 dB-compression point than that of the normal LNA, the gain being higher by 1.7 dB.

CONCLUSION

A 1.9 GHz low noise amplifier fabricated with a conventional digital 0.35 µm SOI CMOS process has been proposed. By using active-body control, it can operate at below 1.0 V with a higher gain and a higher 1 dB-compression point. The gain of 7.0 dB, the NF of 3.6 dB and the input 1 dB-compression point of -4.5 dBm were obtained at 1.0 V.

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REFERENCES

[1] T. Tsukahara, et al., "A 2-V 2-GHz Si-Bipolar Direct-Conversion Quadrature Modulator," IEEE J. Solid-State Circuits, vol. 31, no. 2, pp. 263-267, Feb., 1996.

[2] H. Sato, et al., "A 1.9 GHz Single Chip IF Transceiver for Digital Cordless Phones," ISSCC Digest of Technical Papers, pp. 342-343, Feb., 1996.

[3] C. Takahashi, et al., "A 1.9 GHz Si Direct Conversion Receiver IC for QPSK Modulation Systems," ISSCC Digest of Technical Papers, pp. 138-139, Feb., 1995.

[4] N. Suematsu, et al., "L-Band Internally Matched Si-MMIC Front-End", IEEE Trans. Microwave Theory and Techniques, vol. 44, no. 12, pp. 2375-2378, Dec. 1996.

[5] S. Maeda, et al., "A Highly Reliable 0.35 µm Field Shield Body-Tied SOI Gate Array for Substrate-Bias-Effect Free Operation", Symp. on VLSI Tech. Digest of Technical Papers, pp. 93-94, Jun. 1997.